a graphical controller connected to said core controller and said bus bridge and adapted to be connected to the monitor;

a unified memory control unit including: a graphical-memory address/data path connected to said graphical controller; a system-memory address/data path connected to said core controller; a centralized memory arbiter connected to said core controller and said graphical controller so as to detect a respective memory request signal therefrom; and a unified memory controller adapted to be connected to the system memory and connected to said graphical-memory and system-memory address/data paths, said unified memory controller being further connected to and controlled by said memory arbiter so as to be adapted to allocate access of the system memory to one of said graphical controller and said core controller via a corresponding one of said address/data paths in accordance with status of the memory request signals received by said memory arbiter ; and

three separate and concurrently operable internal buses that connect said graphical controller and a respective one of said core controller, said bus bridge and said unified memory control unit.

A1 CONCL.

2. The integrated circuit device as claimed in Claim 1, wherein said core controller, said bus bridge, said graphical controller and said unified memory control unit are built into a single integrated circuit package.

3. (Canceled)

3 ~~4~~. (Amended) The integrated circuit device as claimed in Claim 1, wherein said internal buses run at the same clock domain as the host bus.

4 ~~5~~. (Amended) An integrated circuit device for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory, said integrated circuit device comprising:

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a core controller adapted to be connected to the host bus;

a bus bridge connected to said core controller and adapted to be connected to the input/output bus;

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a graphical controller connected to said core controller and said bus bridge and adapted to be connected to the monitor;

a unified memory control unit including: a graphical-memory address/data path connected to said graphical controller; a system-memory address/data path connected to said core controller; a centralized memory arbiter connected to said core controller and said graphical controller so as to detect a respective memory request signal therefrom; and a unified memory controller adapted to be connected to the system memory and connected to said graphical-memory and system-memory address/data paths, said unified memory controller being further connected to and controlled by said memory arbiter so as to be adapted to allocate access of the system memory to one of said graphical controller and said core controller via a corresponding one of said address/data paths in accordance with status of the memory request signals received by said memory arbiter;

a first internal bus that interfaces said core controller and said bus bridge;

a second internal bus that interfaces said graphical controller and said core controller;

a third internal bus that interfaces said graphical controller and said bus bridge;

a fourth internal bus that interfaces said graphical controller and said unified memory control unit; and

a fifth internal bus that interfaces said core controller and said unified memory control unit.

5. ~~6.~~ The integrated circuit device as claimed in Claim 4 ~~5~~, wherein said first, second, third, fourth and fifth internal buses are separate from each other and are operable concurrently.

6. ~~7.~~ The integrated circuit device as claimed in Claim 4 ~~5~~, wherein said first, second, third, fourth and fifth internal buses run at the same clock domain as the host bus.

7. ~~8.~~ (New) The integrated circuit device as claimed in Claim 4 ~~5~~, wherein said core controller, said bus bridge, said graphical controller and said unified memory control unit are built into a single integrated circuit package.